6-Bit Flash ADC

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***Abstract*—This project presents a 6-Bit Flash ADC using 45nm technologies in Cadence Virtuoso. The design is composed of three main parts, a resistor ladder, a dynamic comparator ladder, and an encoder. These three components in tandem will allow the device to convert a rail-to-rail analog voltage into a digital value, with a high speed sample rate of over $500MS/s$ and an average power consumption of less than $1mW$.**

***Index Terms*—Flash ADC, Low Power, High Speed, 45nm CMOS**

I. Introduction

For this 6-bit design, 63 parallel comparator stages are necessary, making the high sampling rates and strict power constraints a hurdle. This project implements a 6-bit Flash ADC in 45nm CMOS technology capable of achieving a sampling speed of $500MS/s$ while maintaining power dissipation below $1mW$.

The foundation of this project is informed by the work by Pavan et al., which achieved a highly efficient design by restructuring the encoder [1]. By utilizing a 2:1 multiplexer built with transmission gate and pass-transistor logic, they drastically reduced the transistor count, resulting in a power consumption of just $2.7nW$ for a 5-bit ADC. However, their reliance on static amplifiers limited their maximum sampling speed to approximately $6MS/s$.

To contextualize these metrics, high-speed implementations in older technology nodes, such as a 6-bit Flash ADC in a 180nm CMOS process, have successfully reached speeds of $400MS/s$ but at a much higher power costs of $16.64mW$ [2].

The proposed design merges the advantages of both approaches. It uses the inherent power efficiency of the 45nm node and the optimized logic encoder [1], to minimize power. To elevate the sampling rate to the target without exceeding the $20mW$ limit, the static amplifiers are replaced with dynamic comparators necessary for high-speed analog performance.

II. Proposed Technique

The design consists of three overarching components, which are a resistor ladder, a comparator ladder, and finally, an encoder.

A. Resistor Ladder

The resistor ladder exists to divide the voltage range into equal portions. With 63 equally valued resistors in series, we created 64 voltages, starting at 0V all the way till 1V, with $1/64V$ increments.

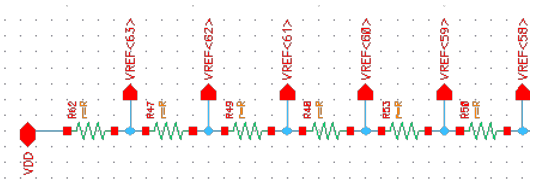


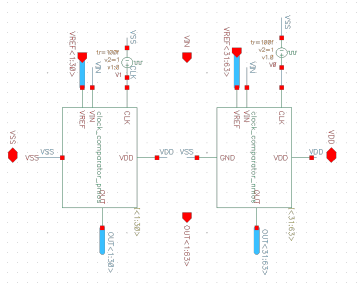
Fig. 1: Resistor Ladder

The selected resistor value for the final design was 30Ω, as a balance of the tradeoffs between RC kickback delay and V^2/R losses. The power dissipated by the ladder is as $P = V_{DD}^2/R_{total} = 1^2/1890 \approx 529\mu W$. This is the majority of the ADC's static power, while maintaining an RC time constant, $\tau \approx (R_{total}/4) \cdot C_{load}$, small enough to rapidly settle kickbacks.

B. Comparator Ladder

The outputs of the resistor ladder has created evenly separated voltages that we can use as references for a ladder of comparators. Connecting the input voltage to each of the comparators, allows us to create a 63-bit thermometer code (e.g., an input at level 3 yields $00\ldots00111$). The proposed comparator ladder achieves rail-to-rail support by utilizing NMOS-tail comparators for reference voltages above 0.5V and PMOS-tail comparators for those below.

StrongARM Latches: To optimize speed and power, the design uses dynamic StrongARM latches paired with trailing set-reset (SR) latches to hold the valid logic state throughout the clock cycle. A StrongARM latch samples a small differential input and uses a cross-coupled inverter pair to exponentially amplify that difference into full-swing digital signals. This dynamic, positive-feedback architecture is significantly faster and more power-efficient than static comparators because it forces a rapid rail-to-rail transition and only draws current during brief switching transients, avoiding continuous static bias [3].



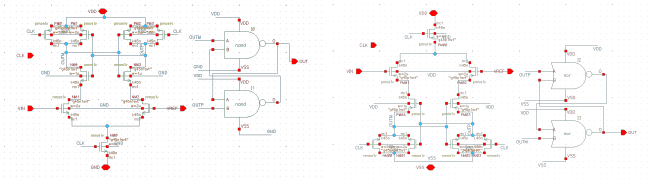


Fig. 2: Comparator Ladder (Top), NMOS-tail comparator (Left), PMOS-tail comparator (Right)

In 1V, 45nm technology, standard threshold voltages range from 0.3V to 0.4V. An NMOS-tail topology requires a minimum input common-mode voltage to ensure both the input pair and tail transistor maintain adequate gate overdrive:

$$V_{CM,min} = V_{TH,N} + V_{DSAT,tail}$$

Conversely, a PMOS-tail architecture evaluates relative to the positive supply and requires a maximum input common-mode voltage to keep its devices actively conducting:

$$V_{CM,max} = V_{DD} - |V_{TH,P}| - |V_{DSAT,tail}|$$

Because of these fundamental headroom limits, an NMOS-tail topology becomes starved of overdrive at inputs below 0.5V, while a PMOS-tail topology degrades at inputs approaching 1V. Utilizing PMOS-tail latches below the 0.5V midpoint and NMOS-tail latches above it guarantees rapid, high-gain evaluation across the entire voltage range without severe offset or delay penalties.

C. Encoder

The encoder employs a cascading "folding" architecture that systematically halves the thermometer code across successive layers. For any given layer receiving an array of inputs (K), the exact middle bit, located at index $(K+1)/2$, acts as the shared select line (S) for every multiplexer in that stage. This middle bit effectively bisects the remaining input signals into a lower and upper half. Each multiplexer then pairs the i-th signal of the lower half (Input B, active when $S = 0$) with the corresponding signal of the upper half (Input A, active when $S = 1$). This folding action produces a new, perfectly scaled-down thermometer code that routes directly into the next layer. The complete schematic is shown in Fig. 4 below.

Decoding a thermometer signal is effectively a binary search. Checking the middle bit immediately determines if the total encoded value reaches the upper half of that layer's specific range, which exactly corresponds to a logic '1' for that binary weight. The subsequent folding isolates the remaining signal, passing it to the next layer to evaluate the next lowest bit. Thus, the select lines from each layer directly produce the final output, starting from the Most Significant Bit at the first layer's select line, and progressing sequentially downward. The Least Significant Bit is extracted directly from the output of the multiplexer in the final layer.

Multiplexer: Here, we show the design of the multiplexer used in the proposed architecture:

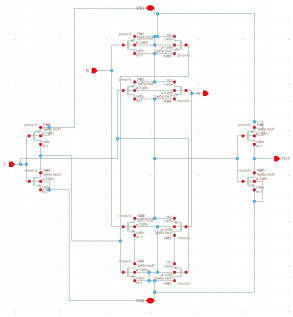


Fig. 3: Multiplexer Schematic

D. Overall Structure

The Flash ADC, on the top level is shown in Fig. 5.

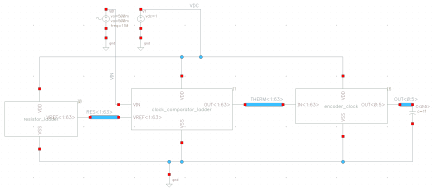


Fig. 5: Top Level Diagram

The resistor ladder output 63 evenly spaced voltages which connect to the 63 comparators in the comparator ladder. With the other input of these comparators being the input voltage to the ADC, the 63 bit thermometer code output of the comparator ladder is subsequently encoded into the 6 bit output which we desire.

III. Simulation Results

The ADC was tested with an $11MHz$ input sin wave, and a sampling rate of $500MS/s$. The following are the simulation outputs:

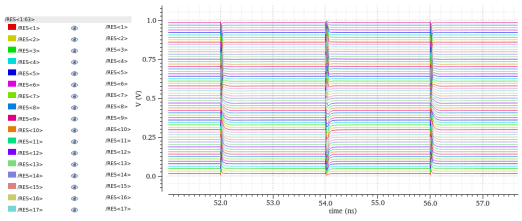


Fig. 6: Resistor Ladder Output

The above simulation demonstrates that while the voltage outputs of the resistor ladder are relatively constant, using dynamic latches causes a certain amount of kickback, preventing us from using arbitrarily large resistor values in the ladder. However, it also demonstrates that with the selected resistance values, the voltage rapidly settles, allowing for precise measurements.

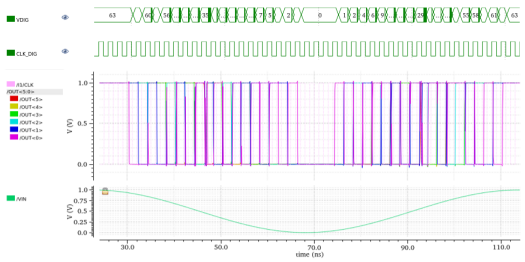


Fig. 7: Accuracy demonstration

The above results compare the digital outputs with the analog inputs, proving that the ADC is indeed accurate across voltages and for the entire rail.

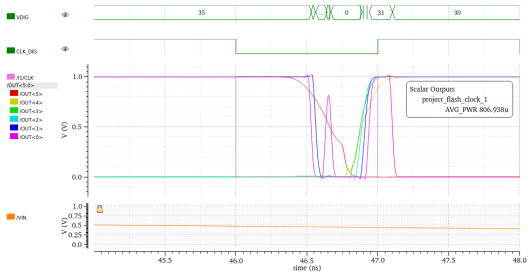


Fig. 8: Frequency demonstration

We selected the transition with the worst latency in the simulation, and found it to be $1.07ns$. This leaves us with considerable leeway before the value is actually sampled, which is at the $2ns$ mark, proving that the design can succesfully run at $500MS/s$.

Finally, the average power, according to the simulation, at a frequency of $500MS/s$ was calculated to be $806.938\mu W$.

IV. Comparative Analysis

In this section, we compare our results with other designs:

	Proposed	Pavan [1]	Tri Vo [2]
Technology	$45nm$	$45nm$	$180nm$
Resolution	6-bit	5-bit	6-bit
Frequency	500MS/s	6MS/s	400MS/s
Power	$809\mu W$	$2.736nW$	$16.64mW$

TABLE I: Performance Comparison

As summarized in the table, the proposed 6-bit Flash ADC demonstrates a highly competitive balance of speed and power efficiency when evaluated against existing literature. Compared to the 45 nm design by Pavan et al., the proposed architecture achieves a significantly higher sampling rate of 500 MS/s and an increased 6-bit resolution, trading off their ultra-low 2.736 nW power footprint for high-speed dynamic performance at 809 µW. Furthermore, when compared to the 6-bit, 180 nm implementation by Tri Vo et al., the proposed design illustrates the benefits of technology scaling and architectural optimization, by successfully exceeding the 400 MS/s sampling speed while achieving a drastic reduction in power dissipation, dropping from 16.64 mW down to under 1 mW.

V. Summary and Conclusion

In this project, a 6-bit Flash ADC was successfully designed and simulated using 45nm CMOS technology. By combining a split NMOS/PMOS dynamic StrongARM comparator ladder with a folding multiplexer-based encoder, the architecture resolves the traditional Flash ADC bottleneck between speed and power. The implementation achieves a high sampling rate of 500 MS/s and maintains full rail-to-rail input functionality, while restricting average power dissipation to just $809\mu W$. These results not only satisfy but significantly exceed the initial design constraints of 100 MS/s and 20 mW. Ultimately, this design demonstrates that leveraging the inherent efficiencies of deep submicron technology alongside targeted digital and analog architectural optimizations allows for massive reductions in power without sacrificing high-speed dynamic performance.

References

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[2] T. Tri Vo, et al. "A 6-bit Low-Power High-Speed Flash ADC using 180 nm CMOS process," *Science & Technology Development*, 2014.

[3] A. Alshehri, et al., "StrongARM Latch Comparator Performance Enhancement by Implementing Clocked Forward Body Biasing," *2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2018. [Online]. Available: http://dx.doi.org/10.1109/icecs.2018.8617903

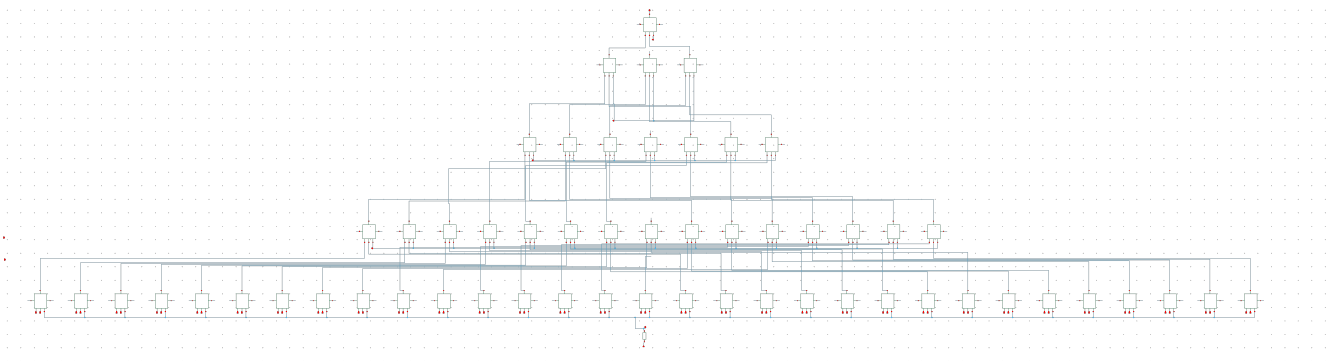

Fig. 4: Encoder Schematic